AMENDMENTS TO THE SPECIFICATION

Please amend the first paragraph on page 2 under the subheading "CROSS-REFERENCE TO RELATED APPLICATION" as follows:

The present application is a divisional of application Serial No. 10/066,668, filed on February 6, 2002, which issued as U.S. Patent No. 6,661,085 on December 9, 2003, the contents of which are incorporated by reference herein.

Please amend third paragraph starting on page 3 as follows:

Existing multi-chip module (MCM) technology is known to provide performance enhancements over single chip or chip-on-chip (COC) packaging approaches. For example, when several semiconductor chips are mounted and interconnected on a common substrate through very high density interconnects, higher silicon packaging density and shorter chip-to-chip interconnections can be achieved. In addition, low dielectric constant materials and higher wiring density can also be obtained which lead to ~~the~~ increased system speed and ~~reliability,~~ reliability and ~~the~~ reduced weight, volume, power consumption and heat ~~to be dissipated~~ dissipation for the same level of performance. However, MCM approaches still suffer from additional problems, such as bulky package, wire length and wire bonding that gives rise to stray inductances that interfere with the operation of the system module.

Please amend the first paragraph under the subheading "DETAILED DESCRIPTION" on page 6 as follows:

The present invention is applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices such as smart ~~card~~ cards, cellular ~~phone~~ phones, electronic tags~~,~~ and gaming devices which

may become available as semiconductor technology develops in the future. However, for the sake of simplicity, discussions will concentrate mainly on exemplary use of a dielectric recess for metallic wafer-to-wafer and die-to-die bonding in a three-dimensional (3-D) wafer-to-wafer vertical stack, although the scope of the present invention is not limited thereto.

Please amend the second paragraph under the subheading "DETAILED DESCRIPTION" on page 6 as follows:

Attention now is directed to the ~~drawings~~ drawings, and particularly to FIGS. 1A-1B~~,~~ in which an example three-dimensional (3-D) wafer-to-wafer vertical stack of a single chip (individual die) is illustrated. As shown in FIG. 1A, the 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafer #1110 which includes an active device layer for supporting, for example, one or more microprocessors; wafer #2120 which includes an active device layer for supporting one or more memory devices; and wafer #3130 which includes an active device layer for supporting one or more radio-frequency (RF) or optical communication devices. The bottom wafer 110 is typically thick to support the stacking of the top wafers 120 and 130, while the top wafers 120 and 130 are thinned to minimize interconnection lengths between wafers 110, 120 and 130.

Please amend the first paragraph on page 7 as follows:

In a typical 3-D vertical stack 100 shown in FIGS. 1A-1B, the active device wafers 110, 120 and 130 are bonded using an interlevel dielectric (ILD) layer 102, while all active layers on wafers 110, 120 and 130 may be electrically interconnected using vertical vias 104. The dielectric (ILD) layer 102 may be a dielectric glue or a polymer ~~adhesive~~ adhesive, such as polyimide and epoxy, to bond wafers 110, 120 and 130 at a low curing temperature ranging from 150 to 400° ~~C~~C, for example, while maintaining electrical isolation between active IC devices of silicon (Si) wafers 110, 120 and 130.

However, other bonding ~~adhesive~~ adhesives such as borophosphosilicate glass (BPSG) may also be used to facilitate the wafer bonding process. Interwafer vias 104 may then be etched through the ILD at arbitrary locations, the thinned top Si wafers 120 and 130, and the cured dielectric layer 102 ~~for providing~~ to provide vertical electrical interconnects between active IC devices of the bottom wafer 110 and the top wafers 120 and 130.

Please amend the second paragraph on page 7 as follows:

Typically, the interwafer vias 104 are prepared on the top wafer 120 as shown in FIG. 1B, for example, by etching through the dielectric (ILD) layer 102. The top wafer 120 is then adhesively bonded to the handling bottom wafer 110 and thinned with high uniformity until ~~the~~ trenches are opened. After the bonding process, the bottom wafer ~~100~~ 110 may be removed, leaving the desired wafer stack that can be further processed like a standard silicon (Si) wafer. The interwafer vias 104 are opened to a standard metallization (typically using Aluminum "Al") and passivation.

Please amend the first paragraph on page 8 as follows:

In order to reduce the use of dielectric (ILD) layers 102 between adjacent wafers 110, 120 and 130, and to minimize the interconnect RC delay in active IC devices through the interwafer vias ~~106~~ 104, proposals have been made to use metallic lines (metal bonding pads) arranged on the surface of adjacent wafers 110, 120 and 130 to serve not only as electrical connections to active IC devices on adjacent wafers 110, 120 and 130 on a 3-D wafer-to-wafer vertical stack 100 but also to bond the adjacent wafers 110, 120 and 130. In addition, dummy metal bonding pads can also be made to increase the surface area for wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active IC devices.

Please amend the first paragraph on page 11 as follows:

As shown in FIGS. 5A-5B, a barrier structure 520 can be advantageously erected on an outer edge of the bonded wafers ~~400A-400B~~ 500A-500B to protect internal die 510A-510N such as die #1 to #16 from corrosion and contamination caused by wafer thinning techniques or generated by other processing steps after the wafers are bonded, and to provide additional structural support for crack propagation control when the bonded wafer pair 500 is cut into individual die. Such a barrier structure 520 may be patterned in the same litho step as the metal bonding pads and use the area on the outer edge of the wafer pair 500 that is unsuitable for die. In addition, the barrier structure 520 can be constructed in the same manner as the metal bonding pads including the dielectric recess, and the surface preparation prior to the metal bonding process so that the wafers ~~400A-400B~~ 500A-500B are also bonded together at the wafer edges.

Please amend the second paragraph on page 12 as follows:

For example, FIG. 6 illustrates an example bonded wafer pair 600 including a plurality of individual die 610A-610N and a barrier structure 620 on an outer edge of individual die pair 610 according to an embodiment of the present invention. FIG. 7 illustrates an example individual die pair 610 including a barrier structure 620 on an outer edge of bonded die according to an embodiment of the present invention. As shown in FIG. 7, the die pair 610 ~~including~~ includes the bottom wafer 710 and the top wafer 720 each of which contains an identical set of metallic lines (metal bonding pads) 730A-730N arranged on opposing surfaces of adjacent wafers 710 and 720 to serve not only as electrical connections to active IC devices on adjacent wafers 710 and 720 but also to bond the adjacent wafers 710 and 720. Each of the adjacent wafers 710 and 720 also contains one or more barrier lines deposited on the perimeter of the die which, when the wafers 710 and 720 are bonded, form a barrier structure 620 to confine the oxidation of exposed metal bonding pads and to provide for additional mechanical strength near the saw cut as shown in FIG. 8.

Please amend the first paragraph on page 14 as follows:

As described in this invention, the barrier structure as shown in FIGS. 5A-5B and 6-8 according to an embodiment of the present invention can be erected, independently or in combination, for both the bonded wafer pair or individual die pair to effectively protect internal die from corrosion and contamination caused by wafer thinning techniques or generated by other processing steps after the wafers are bonded, and to provide additional structural support for crack propagation control when the bonded wafer pair ~~500~~ is cut into individual die.